EAST SEARCH

6/28/02

L#	Hits	Search String	Databases
L1	35	(simulat$6 or model$5) and (hierarch$5 adj analys$3)	USPAT; EPO; JPO; DERWENT; IBM_TDB
L2	33	(circuit$5) and (hierarch$5 adj analys$3)	USPAT; EPO; JPO; DERWENT; IBM_TDB
L3	2	703/$.ccls. and (hierarch$5 adj analys$3)	USPAT; EPO; JPO; DERWENT; IBM_TDB

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Results of search set L1:

US 6408266 B1	Didactic and content oriented word processing method with incrementally changed belief system	20020618	704/1
US 6378123 B1	Method of handling macro components in circuit design synthesis	20020423	716/18
US 6324656 B1	System and method for rules-driven multi-phase network vulnerability assessment	20011127	714/37
US 6321338 B1	Network surveillance	20011120	713/201
US 6303297 B1	Database for storage and analysis of full-length sequences	20011016	435/6
US 6301700 B1	Method and apparatus for slicing class hierarchies	20011009	717/116
US 6295636 B1	RTL analysis for improved logic synthesis	20010925	716/18
US 6292931 B1	RTL analysis tool	20010918	716/18
US 6289498 B1	VDHL/Verilog expertise and gate synthesis automation system	20010911	716/18
US 6289491 B1	Netlist analysis tool by degree of conformity	20010911	716/5
US 6263483 B1	Method of accessing the generic netlist created by synopsys design compilier	20010717	716/18

US 6249902 B1	Design hierarchy-based placement	20010619	716/10
US 6226634 B1	Association rule generation and group-by processing system	20010501	707/4
US 6225025 B1	Fabrication process of a semiconductor device by electron-beam lithography	20010501	430/296
US 6205572 B1	Buffering tree analysis in mapped design	20010320	716/5
US 6179491 B1	Method and apparatus for slicing class hierarchies	20010130	717/116
US 6173435 B1	Internal clock handling in synthesis script	20010109	716/18
US 6075875 A	Segmentation of image features using hierarchical analysis of multi-valued image data and weighted averaging of segmentation results	20000613	382/107
US 6066179 A	Property estimation of an integrated circuit	20000523	716/4
US 6009252 A	Methods, apparatus and computer program products for determining equivalencies between integrated circuit schematics and layouts using color symmetrizing matrices	19991228	716/5
US 5983020 A	Rule-based engine for transformation of class hierarchy of an object-oriented program	19991109	717/141
US 5929940 A	Method and device for estimating motion between images, system for encoding segmented images	19990727	348/699
US 5830657 A	Method for single-tube sequencing of nucleic acid polymers	19981103	435/6
US 5789168 A	Method for amplification and sequencing of nucleic acid polymers	19980804	435/6
US 5692160 A	Temperature, process and voltage variant slew rate based power usage simulation and method	19971125	703/23
US 5692160 A	Power usage simulator for generating baseline power usage model for cells in circuit cell library - bases model on signal slew rates and output load for given baseline temp., supply voltage and process configuration	19971125	
US 5625803 A	Slew rate based power usage simulation and method	19970429	703/14
US 5583995 A	Apparatus and method for data storage and retrieval using bandwidth allocation	19961210	709/219
US 5431011 A	Catalytic converter diagnostic	19950711	60/274
US 5305395 A	Exhaustive hierarchical near neighbor operations on an image	19940419	382/205
US 5280547 A	Dense aggregative hierarhical techniques for data analysis	19940118	382/302
US 5231676 A	Hierarchical operations on border attribute data for image regions	19930727	382/240
US 4706212 A	Method using a programmed digital computer system for translation between natural languages	19871110	704/2
KR 2001095369 A	On-off line auction to internet domain and method for creating profit structure by analyzing business concept to domain	20011107	
JP 63104178 A	NUMERICAL SIMULATION DEVICE	19880509	